

IN THE CLAIMS

Claim 1 (Previously Presented): A reference power supply circuit comprising:

 a first PN junction configured to connect an N type semiconductor area to a first potential;

 a second PN junction configured to connect an N type semiconductor area to the first potential and having a size different from that of the first PN junction;

 a first current supply configured to be connected between a second potential and a P type semiconductor area of the first PN junction, the first current supply supplying a current only to the first PN junction;

 a first resistive element configured to have one end connected to a P type semiconductor area of the second PN junction;

 a second resistive element configured to be connected in parallel with the first resistive element and second PN junction;

 a second current supply configured to be inserted between the other end of the first resistive element and the second potential;

 a third current supply configured to be connected between the second potential and an output terminal; and

 a differential amplifier configured to have an inverting input terminal and a non-inverting input terminal and to receive, at the inverting input terminal, a potential on a first connection point between the first current supply and the first PN junction and, at the non-inverting input terminal, a potential on a second connection point between the second current supply and the first resistive element and to control the first, second and third current supplies

by a difference between a potential of the inverting input terminal and a potential of the non-inverting input terminal.

Claim 2 (Original): A circuit according to claim 1, wherein the differential amplifier has a source follower circuit configured to receive potentials on the first and second connection points.

Claim 3 (Original): A circuit according to claim 1, wherein the size of the second PN junction is greater than that of the first PN junction.

Claim 4 (Original): A circuit according to claim 1, wherein the resistive value of the second resistive element is greater than that of the first resistive element.

Claim 5 (Original): A circuit according to claim 1, further comprising a third resistive element configured to be connected between the output terminal and the first potential, the output terminal outputting a reference voltage.

Claim 6 (Original): A circuit according to claim 1, further comprising a current mirror circuit configured to be connected between the third current supply and the first potential and to output a reference current.

Claim 7 (Original): A circuit according to claim 2, further comprising a bias circuit configured to be controlled by a voltage on the output terminal and to apply a bias potential to the differential amplifier.

Claim 8 (Original): A circuit according to claim 2, further comprising a capacitive load configured to be connected between an output terminal of the differential amplifier and the second potential.

Claim 9 (Currently Amended): A reference power supply circuit comprising:

- a first diode having a cathode connected to a first potential;
- a second diode having a cathode connected to the first potential and having a size different from that of the first diode;
- a first transistor of a first conductivity type configured to be connected between a second potential and the anode of the first diode, the first transistor supplying a current only to the first diode;
- a first resistive element having one end connected to the anode of the second diode;
- a second resistive element configured to be connected in parallel with the first resistive element and second diode;
- a second transistor of a first conductivity type configured to be inserted between the other end of the first resistive element and the second potential and constitute a current supply;
- a third transistor of a first conductivity type configured to be connected between the second potential and an output terminal and constitute a current supply; and
- a source follower differential amplifier having an inverting input terminal and a non-inverting input terminal and configured to receive, at the inverting input terminal, a potential on a first connection point between the first transistor and the first diode and, at the non-inverting input terminal, a potential on a connection point between the second transistor and

the first resistive element, the source follower differential amplifier being configured to control the first, second and third transistors by a difference between a potential of the inverting input terminal and a potential of the non-inverting input terminal.

Claim 10 (Currently Amended): A circuit according to claim 9, wherein the source follower differential amplifier comprises:

a fourth transistor of a first conductivity type having a current path with one end connected to the first potential and a gate connected to the first connection point;

a fifth transistor of a first conductivity type having a current path with one end connected to the first potential and a gate connected to the second connection point;

a sixth transistor of a first conductivity type having a current path with one end connected to the other end of the current path of the fourth transistor and with the other end connected to the second potential, the gate of the sixth transistor being connected to a first output terminal of the bias circuit;

a seventh transistor of a first conductivity type having a current path with one end connected to the other end of the current path of the fifth transistor and with the other end connected to the second potential, the gate of the seventh transistor being connected to the first output terminal of the bias circuit;

an eighth transistor of a second conductivity type having a current path with one end connected to the first potential and a gate connected to a second output terminal of the bias circuit;

a ninth transistor having a current path with one end connected to the other end of the current path of the eighth transistor and a gate connected to the other end of the current path of the eighth transistor;

a tenth transistor of a second conductivity type having a current path with one end connected to the other end of the current path of the eighth transistor and a gate connected to the other end of the current path of the fifth transistor;

an eleventh transistor of a first conductivity type having a current path with one end connected to the other end of the current path of the ninth transistor and said output end and with the other end connected to the second potential; and

a twelfth transistor of a first conductivity type having a current path with one end connected to the other end of the current path of the tenth transistor and with the other end connected to the second potential, the gate of the twelfth transistor being connected to the gate of the eleventh transistor and to the other end of the current path of the tenth transistor.

Claim 11 (Original): A circuit according to claim 9, wherein the size of the second diode is greater than that of the first diode.

Claim 12 (Original): A circuit according to claim 9, wherein the resistive value of the second resistive element is greater than that of the first resistive element.

Claim 13 (Original): A circuit according to claim 9, further comprising a third resistive element connected between said output terminal and the first potential, said output terminal outputting a reference voltage.

Claim 14 (Original): A circuit according to claim 9, further comprising a current mirror circuit connected between said third current supply and the first potential and configured to output a reference current.

Claim 15 (Original): A circuit according to claim 9, wherein said bias circuit comprises a thirteenth transistor of a second conductivity type and fourteenth transistor of a first conductivity type configured to be series-connected between the first potential and the second potential and the gate of the fourteenth transistor being connected to a connection point between the thirteenth transistor and the fourteenth transistor and constituting said output terminal;

a fifteenth transistor of a second conductivity type having a current path with one end connected to the first potential, the gate of the fifteenth transistor being connected to the gate of the thirteenth transistor and to the other end of the current path of the fifteenth transistor and constituting said second output terminal; and

a fourth resistive element having one end connected to the other end of the current path of the fifteenth transistor and the other end connected to the second potential.

Claim 16 (Original): A circuit according to claim 15, wherein said bias circuit comprising a sixteenth transistor of a second conductivity type and seventeenth transistor of a first conductivity type configured to be series-connected between the first potential and the second potential, the gate of the seventeenth transistor being connected to said output terminal of the differential amplifier and constituting said first output terminal and the gate of the sixteenth transistor being connected to a connection point between the sixteenth transistor and the seventeenth transistor and constituting said output terminal.

Claim 17 (Original): A circuit according to claim 10, further comprising a capacitive load connected between an output terminal of the differential amplifier and the second potential.

Claim 18 (Currently Amended): A reference power supply circuit comprising:

- a first PN junction configured to connect an N type semiconductor area to a first potential;
- a second PN junction configured to connect an N type semiconductor area to the first potential and having a size different from that of the first PN junction;
- a first resistive element having one end connected to a P type semiconductor area of the second PN junction;
- a second resistive element configured to be connected in parallel with the first resistive element and said second PN junction;
- a current supply connected between a second potential and an output terminal, the current supply having a control gate; and
- a mirror circuit having first, second, third and fourth nodes, the first node being connected to a P type semiconductor area of the first PN junction, the second node being connected to another end of the first resistive element, the third node being connected to the control gate of the current supply and the fourth node being connected to the second potential, said mirror circuit configured to allow a current which flows through the first PN junction to be copied to a corresponding current through the first and second resistive elements and second PN junction and to control the current supply in accordance with the current through the first and second resistive elements and second PN junction.

Claim 19 (Original): A circuit according to claim 18, wherein the size of the second PN junction is greater than that of the first junction.

Claim 20 (Original): A circuit according to claim 18, wherein the resistive value of the second resistive element is greater than that of the first resistive element.

Claim 21 (Currently Amended): A circuit according to claim 18, wherein the ~~current~~ mirror circuit comprises:

a first transistor has a first gate and a first current path, one end of the first current path is ~~connected to the current supply and another end of the first current path is connected to a P type area of the first PN junction~~ first node, the first transistor supplies a current only to the first PN junction; and

a second transistor has a second gate and a second current path, the second gate is connected to the first gate of the first transistor and ~~one~~ another end of the first current path of the first transistor, and ~~the~~ one end of the second current path is connected to ~~the current supply~~ the second node and another end of the second current path is connected to ~~the first and second resistive elements~~ the third node.